I CLAIM:

1. A method of fabricating switching devices for integrated circuits, comprising:

forming a bottom electrode in contact with a conductive region in a semiconductor base material;

providing a glass electrolyte layer having metal ions diffused therein and being capable of growing conductive paths under the influence of an applied voltage;

forming a top electrode layer; and

patterning and etching through the top electrode layer, the glass electrolyte layer and the bottom electrode to define separate pillars of stacked materials.

2. The method of Claim 1, further comprising forming a liner layer of an insulating material that conforms to the pillars and the semiconductor base material after patterning and etching.

3. The method of Claim 2, wherein forming the liner layer comprises depositing silicon nitride.

4. The method of Claim 2, further comprising forming an insulating layer to fill at least the spaces remaining between the separate pillars of stacked materials after forming the liner layer.

5. The method of Claim 4, wherein forming the insulating layer to fill at least the spaces remaining between the pillars comprises depositing silicon oxide from TEOS.

6. The method of Claim 4, further comprising removing at least some of the insulating layer and some of the liner layer to make contact to the top electrode layer.

7. The method of Claim 6, wherein removing at least some of the insulating layer and some of the liner layer to make contact to the top electrode comprises chemical mechanical polishing.

8. The method of Claim 6, wherein removing at least some of the insulating layer and some of the liner layer to make contact to the top electrode comprises dry etching.

9. The method of Claim 1, wherein forming the bottom electrode layer comprises:

forming a layer of polysilicon onto the semiconductor base material;

forming a layer of tungsten nitride over the polysilicon; and

forming a layer of tungsten over the tungsten nitride.

10. The method of Claim 1, wherein providing a glass electrolyte layer having metal ions diffused therein comprises:

depositing a glass layer;

depositing a metal film over the glass layer; and

providing energy to the metal film and the glass layer to cause metal ion diffusion into the glass layer, thereby forming the glass electrolyte layer..

11. The method of Claim 10, wherein depositing the glass layer comprises depositing a chalcogenide glass whose composition is selected from one or more elements of the group consisting of sulfur, germanium, selenium and tellurium.

12. The method of Claim 11, wherein depositing the chalcogenide glass comprises sputtering $Ge_{25}Se_{75}$.

13. The method of Claim 11, wherein depositing the chalcogenide glass comprises evaporating $Ge_{25}Se_{75}$.

14. The method of Claim 10, wherein depositing the metal film comprises depositing a metal selected from the group consisting of Group IB and Group IIB metals.

15. The method of Claim 10, wherein depositing the metal film comprises depositing silver.

16. The method of Claim 10, wherein providing energy to the metal film and the glass layer comprises exposing to ultraviolet radiation.

17. The method of Claim 16, wherein exposing to ultraviolet radiation comprises using ultraviolet radiation with a wavelength of less than 500 nm at about 4 mW/cm^2 for about 15 min.

18. The method of Claim 1, wherein forming the top electrode includes leaving a portion of the metal film over the glass electrolyte layer.

19. The method of Claim 1, wherein forming a top electrode layer comprises deposition of tungsten.

20. The method of Claim 1, wherein patterning comprises photolithographic techniques.

21. The method of Claim 1, wherein etching includes a physical etch component.

22. The method of Claim 21, wherein the etching comprises sputter etching.

23. The method of Claim 21, wherein the etching comprises reactive ion etching.

24. The method of Claim 1, wherein the separate pillars of stacked materials are less than about 250 nm in width.

25. The method of Claim 1, wherein the spaces between separate pillars of stacked materials are at least about 300 nm in width.

26. A method of fabricating programmable conductor memory cells on a substrate by blanket layer deposition, comprising:

forming a bottom electrode layer;

providing a chalcogenide glass layer having metal ions diffused therein and being capable of growing conductive pathways under the influence of an applied voltage;

forming a top electrode layer; and

removing the bottom electrode layer, the chalcogenide glass layer and the top electrode layer together from portions of the substrate, thus leaving individual pillars standing separately on the substrate.

27. An array of programmable conductor memories in an integrated circuit comprising pillars of stacked materials on a semiconductor substrate.

28. The array of Claim 27, wherein the regions between the pillars comprise insulating material.

29. The array of Claim 28, wherein the insulating material comprises silicon oxide.

30. The array of Claim 29, wherein the silicon oxide comprises tetraethylorthosilicate (TEOS).

31. The array of Claim 29, wherein there is a silicon nitride layer that conforms to the pillars and to the substrate below the silicon oxide.

32. The array of Claim 31, wherein the silicon nitride layer is between 5 nm and 50 nm thick.

33. The array of Claim 26, wherein each pillar comprises:

a bottom electrode;

a body formed of a glass electrolyte layer having metal ions diffused therein; and

a top electrode.

34. The array of Claim 33, wherein the bottom electrode comprises:

a polysilicon layer;

a tungsten nitride layer; and

a tungsten layer.

35. The array of Claim 34, wherein the polysilicon layer is between about 25 nm and 75 nm thick.

36. The array of Claim 34, wherein the tungsten nitride layer is between about 5 nm and 40 nm thick.

37. The array of Claim 34, wherein the tungsten layer is between about 50 nm and 100 nm thick.

38. The array of Claim 33, wherein the glass electrolyte material having metal ions diffused therein comprises a chalcogenide glass.

39. The array of Claim 38, wherein the chalcogenide glass having metal ions therein comprises silver germanium selenide.

40. The array of Claim 39, wherein the silver germanium selenide layer is between about 25 nm and 75 nm thick.

41. The array of Claim 33, wherein the top electrode comprises a tungsten layer.

42. The array of Claim 41, wherein the tungsten layer is between about 5 nm and 25 nm thick.

43. The array of Claim 33, wherein the glass electrolyte material having metal ions therein forms conductive pathways grown from a negative electrode to a positive electrode when a first voltage is applied to the electrodes.

44. The array of Claim 43, wherein the conductive pathways remain stable when voltage is removed from the electrodes.

45. The array of Claim 43, wherein the conductive pathways shrink when a second voltage, opposite in polarity to the first voltage, is applied to the electrodes.

46. A method of fabricating programmable conductor memory cells by blanket layer deposition and post-patterning, comprising:

forming a bottom electrode comprising tungsten in contact with a conductive region in a silicon substrate;

providing a germanium selenide glass layer having silver ions diffused therein;

forming a top electrode layer comprising tungsten;

identifying defined cell regions; and

etching off blanket layers down to the silicon substrate that are not within the defined cell regions.

47. The method of Claim 46, further comprising forming a liner layer of silicon nitride that acts as a diffusion barrier and conforms over the cells and the silicon substrate.

48. The method of Claim 47, further comprising forming an insulating layer to fill at least the spaces between the separate cells.